UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,698	11/19/2003	Gary A. Frazier	004578.1373	6574

7590 07/12/2004

T. Murray Smith, Esq.
Baker Botts L.L.P.
Suite 600
2001 Ross Avenue
Dallas, TX 75201-2980

EXAMINER	
YOUNG, BRIAN K	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,698	FRAZIER, GARY A.	
	Examiner	Art Unit	
	Brian Young	2819	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-9 and 19-24* is/are allowed.

6)☒ Claim(s) *10-12* is/are rejected.

7)☒ Claim(s) *13-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Burns. Burns et al disclose a resonant tunneling diode device in FIG. 5. A differential current driven latch in which the current division between two tunnel diodes is governed by a ***differential*** current supplied by an XOR gate. During a TRACK phase, the currents through both tunnel diodes are supplied by the XOR portion of the gate and kept at relatively low levels within the "tracking region" 10 illustrated in the figure. The connection to the XOR portion of the gate causes the currents through the two diodes to differ, depending upon the input analog signal. When a clock signal is applied to switch the circuit to the LATCH mode, bias current is added to both diodes that brings the higher current diode slightly above Ip, while leaving the current through the other diode slightly below Ip. This brings the higher current diode within the "trigger region" 12 illustrated in the figure. Upon triggering, the ***higher current diode jumps*** from Vp to V1 in the higher voltage region of positive impedance, retaining the same current Ip. This transition occurs extremely rapidly, ***due to the quantum tunneling effect***. The latching circuits are operated in a current mode, with a control circuit providing control currents to the latching devices that rise over non-zero rise times in response to a LATCH signal and add to the differential logic currents from the

XOR portion of the gate. The differential logic currents vary between high and low logic values; the full value of the control current when added to the high logic current level is sufficient to trigger the associated latching device, which in turn causes the other latching device to be held off. The control currents are produced in response to a periodic clock signal that causes the circuit to acquire new input analog samples on the positive edge of each clock pulse at the clock rate.

Since the diode current excursions from the XOR portion of the gate are considerably less than the applied bias current, the current through the triggered diode cannot fall below Iv; the diode therefore latches in a stable triggered state. Furthermore, a cross-coupling circuit described below reduces the current through the non-triggered tunnel diode in response to the positive voltage jump for the triggered diode. This causes the non-triggered device to latch at an operating point below the trigger region 12, so that fluctuations in the current from the XOR circuit cannot thereafter raise its current high enough to trigger. The circuit is thus latched in a stable state, with one tunnel diode held triggered and the other non-triggered, regardless of the changing currents received from the XOR circuit due to the varying input analog signal. The circuit remains in this latched state until it is reset to a TRACK mode by removing the clock signal, at which time the current in the triggered device falls back below Iv until the next clock signal is applied.

3. Claims 1-9 and 19-24 are allowed.

4. Claims 13-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

***